WHAT IS CLAIMED IS:

1. A method of handling instructions within a processor comprising:

decoding at least a portion of an instruction coded in a first code;

re-encoding the at least a portion of the instruction to a second code if necessary; and

forwarding the re-encoded instruction to a destination.

2. The method of Claim 1, further comprising determining the destination of the instruction.

3. The method of Claim 2, further comprising sending at least a portion of the coded instruction to a functional unit.

4. The method of Claim 2, further comprising sending at least a portion of the decoded instruction to a functional unit.

5. The method of Claim 1, further comprising determining a portion of the coded instruction to decode.

6. The method of Claim 1, further comprising forwarding the re-encoded instruction to a functional unit.

7. The method of Claim 1, further comprising handling instructions in a digital signal processor.

8. A method of processing instruction within a processor comprising:

receiving an instruction which is coded in a first code;

determining at least a destination location for the instruction;

forwarding any portion of the coded instruction having a destination location of a first location;

decoding any remaining portion of the instruction;

forwarding any portion of the decoded instruction having a destination location of a second location;

re-encoding any remaining portion of the instruction to a second code if necessary; and

forwarding the re-encoded instruction to a third location.

9. The method of Claim 8, wherein said forwarding steps comprise forwarding the instructions to the first, second and third locations which comprise functional units.

10. The method of Claim 9, further comprising forwarding any portion of the decoded instruction having a destination location of a second location to a data address generator.

11. The method of Claim 9, further comprising forwarding the re-encoded instruction to a system pipe.

12. The method of Claim 8, further comprising processing instructions within a digital signal processor.

13. The method of Claim 8, further comprising decoding and re-encoding with a decoder.

14. A processor comprising:

a decoder which receives an instruction coded in a first code and decodes at least a portion of the instruction;

an encoder which re-encodes the at least a portion of the instruction to a second code.

15. The processor of Claim 14, wherein the decoder determines the destination of the instruction.

16. The processor of Claim 15, wherein the decoder forwards control signals to other portions of the processor.

17. The processor of Claim 16, wherein the control signals may be in the first code or the second code.

18. The processor of Claim 14, wherein the processor is a digital signal processor.